What is claimed is:

1. A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;

a partial-isolation insulating film formed in a main surface of said semiconductor layer;

a first semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

an interlayer insulating film formed on said first semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a first complete-isolation insulating film formed extending from said main surface of said semiconductor layer, reaching an upper surface of said insulating layer below at least one of said power supply line and ground line.

2. The semiconductor device according to claim 1, further comprising:

a second semiconductor element formed adjacently to said first semiconductor element in said semiconductor layer, having an operating threshold voltage different from that of said first semiconductor element; and

a second complete-isolation insulating film formed extending from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer between said first semiconductor element and said second semiconductor element.

3. The semiconductor device according to claim 1, further comprising:

a second semiconductor element formed adjacently to said first semiconductor element in said semiconductor layer, having an operating frequency different from that of said first semiconductor element; and

a second complete-isolation insulating film formed extending from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer between said first semiconductor element and said second semiconductor element.

4. The semiconductor device according to claim 1, further comprising:

a signal line formed on said interlayer insulating film, being electrically connected to said first semiconductor element; and

a second complete-isolation insulating film formed extending from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer below said signal line.

5. The semiconductor device according to claim 4, wherein

said signal line is made of metal.

6. The semiconductor device according to claim 4, wherein

said signal line is made of polysilicon.

7. The semiconductor device according to claim 1, further comprising:

a bonding pad formed on said interlayer insulating film, for electrically connecting said first semiconductor element and an outer element; and

a second complete-isolation insulating film formed extending from said main

surface of said semiconductor layer, reaching said upper surface of said insulating layer below said bonding pad.

8. A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;

a partial-isolation insulating film formed in a main surface of said semiconductor layer;

a semiconductor element formed in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

an interlayer insulating film formed on said semiconductor element and said partial-isolation insulating film; a signal line formed on said interlayer insulating film, being electrically connected to said semiconductor element; and

a complete-isolation insulating film formed extending from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer below said signal input line.

9. The semiconductor device according to claim 8, wherein

said signal line has a plurality of wires constituting a multilayer interconnection structure, and

said complete-isolation insulating film is formed below at least one of said plurality of wires which exists in the lowest layer.

10. The semiconductor device according to claim 9, wherein

said complete-isolation insulating film is also formed below one of said plurality

of wires which exists in the layer nearest to said SOI substrate but said lowest layer.

11. The semiconductor device according to claim 8, wherein

said signal line propagates a signal having a frequency not less than GHz order.

12. The semiconductor device according to claim 8, wherein

said semiconductor element is a buffer circuit, and

said signal line connects said buffer circuit and a bonding pad connected to an external device.

13. A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;

a partial-isolation insulating film formed in a main surface of said semiconductor layer;

a semiconductor element including a channel region formed in said semiconductor layer in an element formation region defined by said partial-isolation insulating film;

an interlayer insulating film formed on said semiconductor element and said partial-isolation insulating film;

at least one of a power supply line and a ground line formed on said interlayer insulating film; and

a high-resistance region formed below at least one of said power supply line and ground line in said semiconductor layer, having a resistance higher than that of said channel region.

14. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order;

(b) forming a partial-isolation insulating film in a main surface of said semiconductor layer and forming a first complete-isolation insulating film so as to extend from said main surface of said semiconductor layer and reach an upper surface of said insulating layer below a region in which at least one of a power supply line and a ground line is to be formed;

(c) forming a first semiconductor element in an element formation region defined by said partial-isolation insulating film in said semiconductor layer;

(d) forming an interlayer insulating film on said first semiconductor element, said partial-isolation insulating film and said first complete-isolation insulating film; and

(e) forming at least one of said power supply line and said ground line on said interlayer insulating film.

15. The method of manufacturing a semiconductor device according to claim 14, further comprising the steps of:

(f) forming a second semiconductor element adjacently to said first semiconductor element in said semiconductor layer, to have an operating threshold voltage different from that of said first semiconductor element; and

(g) forming a second complete-isolation insulating film so as to extend from said main surface of said semiconductor layer and reach said upper surface of said insulating layer between said first semiconductor element and said second semiconductor element.

16. The method of manufacturing a semiconductor device according to claim 14, further comprising the steps of:

(f) forming a second semiconductor element adjacently to said first semiconductor element in said semiconductor layer, to have an operating frequency different from that of said first semiconductor element; and

(g) forming a second complete-isolation insulating film so as to extend from said main surface of said semiconductor layer and reach said upper surface of said insulating layer between said first semiconductor element and said second semiconductor element.

17. The method of manufacturing a semiconductor device according to claim 14, further comprising the steps of:

(h) forming a second complete-isolation insulating film so as to extend from said main surface of said semiconductor layer and reach said upper surface of said insulating layer below a region in which a signal line electrically connected to said first semiconductor element is to be formed; and

(i) forming said signal line on said interlayer insulating film.

18. The method of manufacturing a semiconductor device according to claim 14, further comprising the steps of:

(j) forming a second complete-isolation insulating film so as to extend from said main surface of said semiconductor layer and reach said upper surface of said insulating layer below a region in which a bonding pad for electrically connecting said first semiconductor element and an outer element is to be formed; and

(k) forming said bonding pad on said interlayer insulating film.

19. The method of manufacturing a semiconductor device according to claim 14, wherein

said step (b) has the steps of

(x) excavating said main surface of said semiconductor layer by a predetermined film thickness in a region in which said partial-isolation insulating film is to be formed and a region in which said first complete-isolation insulating film is to be formed, to form a first recess;

(y) selectively excavating a bottom surface of said first recess exposed in said step (x) in said region in which said first complete-isolation insulating film is to be formed until said upper surface of said insulating layer is exposed, to form a second recess; and

(z) burying an insulating film in said first recess and said second recess.

20. The method of manufacturing a semiconductor device according to claim 19, wherein

said step (y) has the steps of

(y-1) forming a photoresist on a structure obtained in said step (x);

(y-2) exposing said photoresist by using a photomask having a predetermined mask pattern;

(y-3) developing said photoresist after being exposed; and

(y-4) etching said semiconductor layer with said photoresist after being developed used as an etching mask, to form said second recess,

and wherein said predetermined mask pattern is automatically formed on the basis of a wiring layout representing a region in which at least one of said power supply

line and said ground line is to be formed.